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EXAMINER	
SILVER, DAVID	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/627,977	WOZNIAK, ANDRZEJ	
	Examiner	Art Unit	
	DAVID SILVER	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *105-118 and 130-143* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *105-118 and 130-143* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 105-118 and 130-143 are currently pending in Instant Application.

2. The Instant Application is not currently in condition for allowance.

Response to Arguments

Response: 35 U.S.C. § 103

3. **Applicants argue:**

However, the cited portions of Yalamanchili and OrCAD fail to teach or suggest generating a simulation model comprising software simulation elements corresponding to an integrated circuit under development. In contrast, the cited portion of Yalamanchili describes a digital system design flow where simulation models are applied to verify the circuit design before manufacture, and the cited portion of OrCAD describes an auto-routing protocol to verify the circuit design before manufacture.

Thus, although Yalamanchili and OrCAD arguably teach performing simulation verification on integrated circuits prior to development, both fail to teach or suggest generating a simulation model comprising software elements corresponding to an integrated circuit under development, as recited in Claim 105. Additionally, although assuming arguendo that it could be obvious to apply a known simulation model to verify the design circuit before it is manufactured, as suggested by the Office Action on page 4, Applicant respectfully submits that it is not obvious to substitute applying a simulation model with generating a simulation model comprising software elements corresponding to an integrated circuit under development. (Remarks: page 3)

4. **Examiner Response:**

Applicants' remarks are at best generally conclusionary statements. Specifically, no analysis was made other than a statement of contrast which merely discusses a single feature of the reference. The conclusion statement is not based on fact findings, but amounts to a general allegation of patentability. The statement of non-obviousness is likewise a general allegation without proper analysis.

Nevertheless, the arguments are traversed and the features are taught as follows. Schubert discloses the said feature in **(para 0178)**: "In case the design instrumentation database is implemented as a software program, its elements (for example, the above-described objects) could be implemented as commands of a computer language. Each command can have one or more arguments to denote the information regarding the associated object. Having a design instrumentation database which can be described in terms of a computer software language has the advantage that such a design instrumentation database can easily be migrated and transported in between a wide variety of different computer systems, as long as the computer system supports the underlying computer software language that the design instrumentation database is written in."

Further, as the Specification of the Instant Application fails to expressly define "software elements", the broadest most reasonable interpretation of any software element, such as, for example, a register, a memory, a language statement, an array, etc. As such, Schubert, Yalamanchili and OrCad individually and in combination all disclose simulation of simulation models, and circuits, the simulators necessarily need to read and execute the model. To do so require software resources (elements) to initialize the features being modeled. As such, it necessarily requires software elements that represent the circuit under development. Thus, this limitation is taught by the references as cited.

Arguments for claim 130 are addressed above.

Compact Prosecution

5. It appears that paragraph 0122 of the Specification contains matter that, if properly claimed, would overcome the prior-art of record and would likely place the Application in condition for allowance. Specifically, the aspects of entries describing the type of connection as direct / not direct in combination with the disclosed two intermediate blocks and their specific head-to-tail configuration.

If any questions should arise, the Applicants are encouraged to contact the Examiner (via phone number provided at the end of this Office Action) for further clarification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 105-118 and 130-143 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schubert **(US 20030069724 A1)**, and in view of Yalamanchili's "VHDL: From Simulation to Synthesis", and further in view of OrCAD's "Autorouter User's Guide".

As per claims 105-118, note the rejection of claims 130-143 below. The Instant Claims recite substantially same limitations as the below-rejected claims and are therefore rejected under same prior-art teachings, except claims 105 recite a "means for" structure, which is disclosed by Schubert as "host computer" in **(para 0011)**, or alternatively, as the "computer readable medium" disclosed in **(para 0028 / 0516)**.

Schubert discloses: 130. (New) A method for automatically generating a simulation model for a selected configuration of software simulation elements, comprising:

storing a plurality of said software simulation elements, said plurality of software simulation elements provided with inter working connections so as to constitute the simulation model of an architecture, each said software simulation element representing a component **(para 135: HDL description and the elements therein, 142, 152, para 122)**;

creating a simulation of wiring by executing stored regular expressions **(para 122)**;

using the configuration definition file, a component and connection rule table, and a connection

coherency rule table, wherein the component and connection rule table and the connection coherency rule table are written in a high level language, and the component and connection rule table describes properties of said software components for simulating at least one of the plurality of integrated circuits **(para 122, 135, 142, 152, 18, 93, 198, 227, 91, 275)**;

instantiating components based on a configuration definition file; and combining, via a high level language (HLL) code generator, the parameters of the components with the connection rules of the component and connection rule table; **(para 85-84)**

automatically generating source code files comprising the simulation model corresponding to the selected configuration specified by the configuration definition file **(para 270, 344)**,

wherein the simulation model comprises software simulation elements each corresponding to an integrated circuit which together comprises the design of a processing machine that conforms to a functional specification of the selected configuration as defined in the configuration definition file **(para 91, 275, 122, 135, 142, 152, 18, 93, 198, 227)**.

Schubert however does not expressly disclose the following features: integrated circuit is under development; and "wherein the integrated circuits are not physically present in the processing machine".

Yalamanchili however discloses an analogous system having the above-mentioned features **(page 7 - top slide)**. Note, for example, the description for manufacture is generated only after simulation, not before.

One of ordinary skill in the art would have been motivated to perform such a combination in order to test the design prior to manufacturing by simulating prior to manufacture, and performing simulation on integrated circuits which are simulation model-based. This would allow engineers to verify performance prior to investment of time and money in circuits. Thus, saving time and money associated with having to remanufacture a circuit with an error. This is further evidenced by OrCAD which demonstrates routing prior to manufacturing **(page 36 - item Auto DFM)** which discloses design before manufacturing.

Schubert discloses: 131. The method according to claim 130, wherein the components comprise Active Components, Monitoring and Verification Blocks, Intermediate Blocks, System Blocks, and Global Blocks **(para 15, 23, 122, 123, 138, 141, 146)**.

Schubert discloses: 132. The method according to claim 131, further comprising performing a conformity check of the connections by comparing an instance connection table with a table of coherency rules for the physical connections between the models chosen from the blocks to constitute the simulation model **(para 150, 163)**.

Schubert discloses: 133. The method according to claim 132, further comprising:

comparing the instance connection table to the connection coherency rule table to detect any incompatible connections between the ends of the connections between blocks **(para 150, 163)**; and

in cases where an incompatible connection is detected, specifying and adding an adapter component (Intermediate Block) to the instance connection table, said adapter component being inserted into the detected incompatible connection between the components **(para 122: "connecting internal signals of a BB to communication ports of the BB and/or connecting internal signals of the BB to communication ports of other BBs in the HDL Design", and para 150, 163, 10)**.

Schubert discloses: 134. The method according to claim 133, wherein the component and connection rule table includes properties of the components and contains parameters common to all of the component types and exists in the form of a table distributed into one or more associative tables, and entries being names designating all possible models for the same component **(Fig 29 and description)**.

Schubert discloses: 135. The method according to claim 134, wherein the associative tables are adapted to contain a description either in the form of parameter sets or in the form of references to procedures that generate a set of values, and wherein entries of the associative tables comprise names each of which designates a possible model for the same component, and form a character string containing predetermined special identifiers that are replaced by calculated values **(Fig 29 and description)**.

Schubert discloses: 136. The method according to claim 135, further comprising:

indicating, using at least three selectors, the instance to be used; and transmitting the following

selectors as parameters to a constructor of an HLL object **(Fig 25 and description)**: a first selector indicating a current instance (item); a second selector specifying the current instance connected to an end of a port; and a third selector indicating a composite instance corresponding to an active Component containing an observation port **(Fig 29 and description)**.

Schubert discloses: 137. The method according to claim 130, further comprising:

representing, by one or more connection coherency rule tables, the rules for interconnecting the components and for inserting intermediate components; representing, by one or more component and connection rule tables, the system- level connection rules and the rules for generating connections between the signals; and representing, by one or more source file formatting tables, the rules for generating instances of HLL objects **(para 170)**.

Schubert discloses: 138. The method according to claim 130, further comprising:

uniquely identifying, via an HLL base class, each object instantiated; generating and automatically instantiating System Blocks; using tables to associate the signals connected together under a unique name of the connecting wires; and using a formatting table to generate the hardware description language and HLL source files **(para 21)**.

Schubert discloses: 139. The method according to claim 130, further comprising:

receiving, from an operator, a functional specification of the configuration in a high level language; and completing the functional specification with the components in a language other than said high level language **(para 88)**.

Schubert discloses: 140. The method according to claim 130, further comprising:

defining, using the following entries in a hash, a Component Type; and correlating, using the following entries in the has, each Component Type to the hash, wherein said hash comprises the following: a first entry comprising a name of a hardware description language (HDL) module of a component and a name of a corresponding source file; and a second entry comprising a definition of a method for selecting the signals that are part of a Port, said definition comprising a set of entries indexed by a name of the Port; wherein said method further includes associating each said Port name with a table

of regular expressions and a pointer to a signal connection procedure that controls the application of the expressions to the names of the signals of the interface of the component **(para 221, 409, 455)**.

Schubert discloses: 141. The method according to claim 140, wherein

said Component Type comprises one or more Active Components having a generic structure that includes a containing Block that contains an HDL Block including an HDL description and a Block in HLL that provides access paths to HDL resources and a description of the containing block in the high level language **(para 15, 92, 99)**;

wherein the set of signals of the HDL Block constitutes an interface of the containing Block, formed by one or more Ports, comprising arbitrary logical selections of signals of an interface, and also formed by interface adapters which provide, in each said Port, two-way communication between the high level language and hardware description language **(para 15, 92, 99)**.

Schubert discloses: 142. A method according to claim 141, further comprising specifying the Ports in the form of regular expressions that select subsets of signals to be connected and define connection rules **(para 15, 92, 99)**.

Schubert discloses: 143. A method according to claim 130, further comprising generating Transfer Components which are inserted to be operable at each side of an interface between servers, said Transfer Components comprising wires for inputs and registers for outputs **(para 15, 92, 99)**.

Conclusion

7. The Instant Application is not currently in condition for allowance.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

/ DS /
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